Amplifier Alphabet Soup: Part II, Basics of Power Amplifier Classes D, E, F and Inverse-F

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1. Introduction

In the last twenty years or so, the increased availability of inexpensive high speed power transistors developed for use in switching power supplies has prompted a revolution in power amplifier design. Voltage regulating switching power supplies avoid the losses encountered in traditional linear "series pass" or shunt regulators by adjusting the on-off transitions of the power transistors; i.e. using the transistors in either a "fully-on" or "fully-off" state to reduce resistive loss. It turns out that these same techniques can yield very efficient power amplifiers as well.

Part I of this series summarized the operation of the classical limited conduction angle amplifier topologies (Class-A, AB, B, C). A common feature of the classical amplifiers is the fact that the transistor spends significant time in its resistive "transition" region as the transistor action tracks the input waveform. This is a source of loss and inefficiency. The "switchers", on the other hand, are designed to swing quickly between a high resistance state to a low resistance state and back again. In this way, little time is spent in the resistive region, thereby maximizing efficiency. The switchers are given the class designators D, E, F and inverse F. Note that switching amplifiers are by definition non-linear with respect to the input signal; that is, amplitude information is not preserved. Various linearization techniques are possible, but that is the possible subject of another article.

As in Part I, we shall focus on a qualitative review of these amplifier class definitions as well as giving some explanation on where inefficiencies appear in each. Some of the advantages and disadvantages of each topology will be presented and the trade-offs will be briefly elaborated in an intuitive manner. The active devices will be assumed to be ideal (i.e. no or only resistive parasitics, no switching delays, etc.) to simplify the exposition. Naturally, the analysis and design of real-world amplifiers must consider the effects of parasitics and imperfections, which are often the major impediment to developing real-world versions of these amplifiers. However, for clarity of exposition, effects of device parasitics and imperfections are ignored in this article.

The topic of input networks is also not covered here since the main focus is on amplifier output class definitions. All efficiencies stated are so-called "collector efficiencies" that do not include input signal power losses. Collector efficiency refers to the efficiency of converting DC supply power into RF power while not saying anything about how much power is needed to drive the amplifier. The reader may be familiar with the notion of power added efficiency (PAE). PAE calculations require knowledge of the input signal environment as well, which is not discussed in detail here. The reader should be aware that final DC to RF conversion

efficiency depends on a number of interacting factors (e.g. the number of stages in the amplifier, the gain and efficiency of each stage, RF input power, etc.). It is hoped, despite some of the simplifying assumptions, that this discussion of amplifier classes can serve readers as a starting point for further investigation into the intricacies of power amplifier design.

2. Switching Amplifiers

2.1. Class-D

The Class-D amplifier represents the simplest form of switching amplifier that usually utilizes so-called "hard-switching" (i.e. switching transitions and output network timing are not coordinated). One of the advantages of Class-D operation is that can simulate linear amplifier operation by means of pulse-width modulation on the input signal. Figure 1 shows a simplified Class-D amplifier with a series resonant output network. This topology is the so-called voltage-mode Class-D amplifier because a constant voltage source is presented to the transformer center tap, hence the load sees the amplifier output as a low-impedance voltage source.

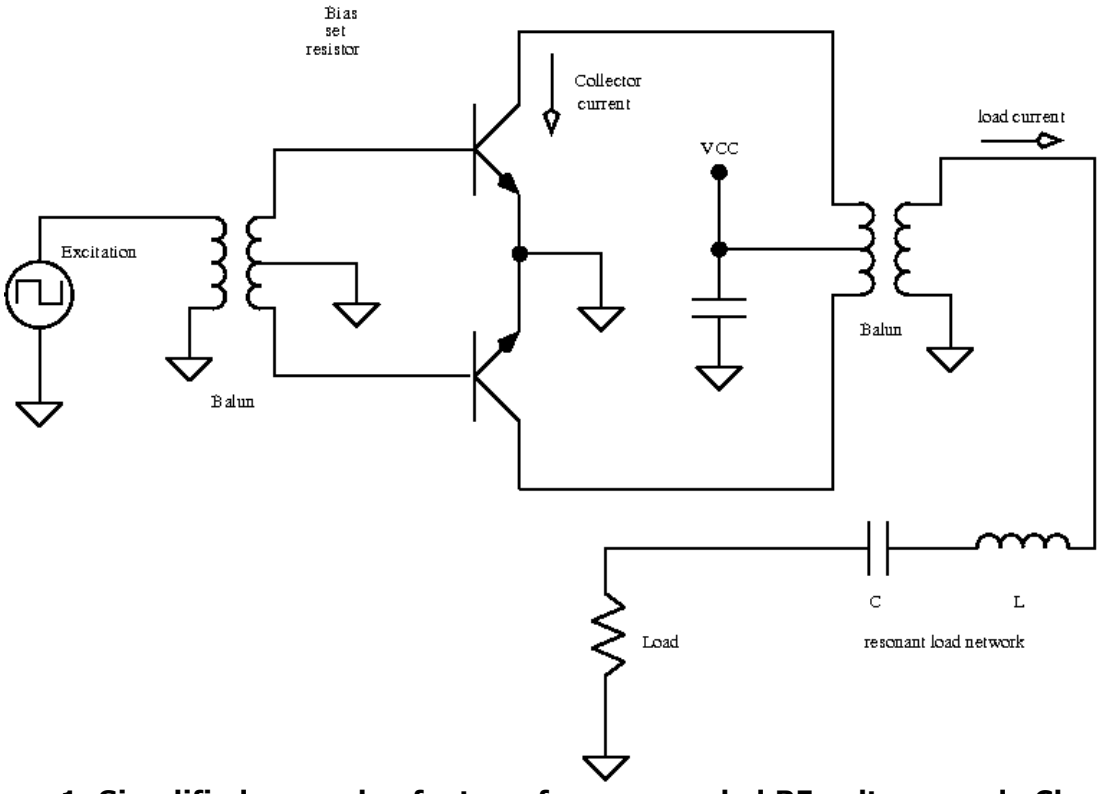

Figure 1: Simplified example of a transformer coupled RF voltage mode Class-D push-pull amplifier

Figure 2, on the other hand, illustrates a current mode Class-D amplifier. The series inductor on the center tap (RFC) of the transformer primary causes the VCC supply to look like a constant current source. As a consequence, looking into the amplifier from the load, we see a high impedance source: i.e. a current source. Hence, a parallel resonant load circuit is appropriate. Figure 2 also shows back-biased diodes across each switching transistor. This is to highlight the fact that current mode switching requires some way to "close the loop" if both switches are simultaneously "off" for some reason ("dead-time", in switch-mode parlance). If a current path is not present, the switching transistors can be subjected to destructively high voltage transients because of the RF choke current that cannot change rapidly.

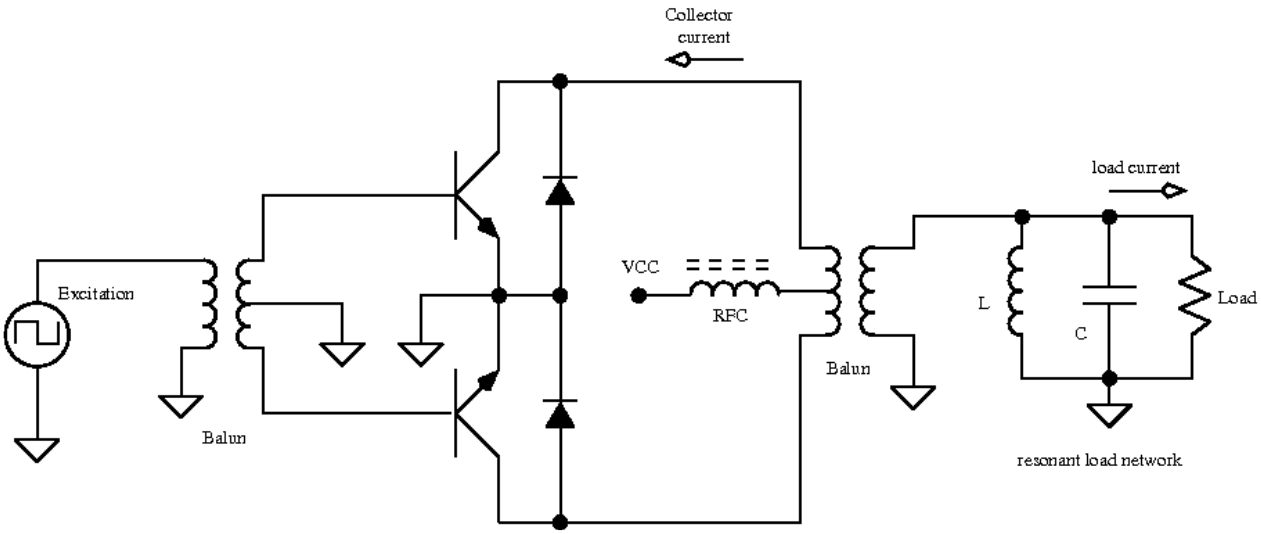

Figure 2: Current mode Class-D amplifier example. Note the series inductor on the transformer center tap and the back-biased diodes on the switches.

For the sake of clarifying the explanation, we can make the simplifying assumption that the for the voltage mode, the resonant network only passes current at the fundamental frequency and looks like an open circuit to all higher order harmonics. For the current mode Class-D, we have the dual situation: the parallel load network "shorts out" higher order harmonics, passing only the fundamental voltage to the resistive load. This assumption is valid in practice for resonant output circuits where the Q is 8-10 or more. We can also assume that the transformers are ideal. However, let us assume a finite transistor "on" resistance. The purpose of this is to show how losses can reduce efficiency, although the maximum theoretical efficiency of this amplifier is 100% (recall the "squared-up" waveform in our previous Class-C explanation).If we allow the transistor to have an on resistance R_{on} that is 10% of the load resistance R_l, the average power loss over a cycle will be 10%. Hence, overall collector efficiency will be 90%.

It should be clear from the collector voltage/current plots in Figure 3 and Figure 4 (for the voltage mode Class-D amp) how this works. Notice that when the transistor is switched on (low V_{ce}), there is a finite voltage across the transistor at the same time as there is current

flowing. The overlap between the voltage and current curves are related to the losses (i.e. the average value of $V_{ce}*I_c$ yields the transistor power loss). Since we also know the current drawn from the DC power supply, efficiency is simple to calculate.

In the current-mode Class-D amplifier, the voltage and current curves in Figure 3 are interchanged.

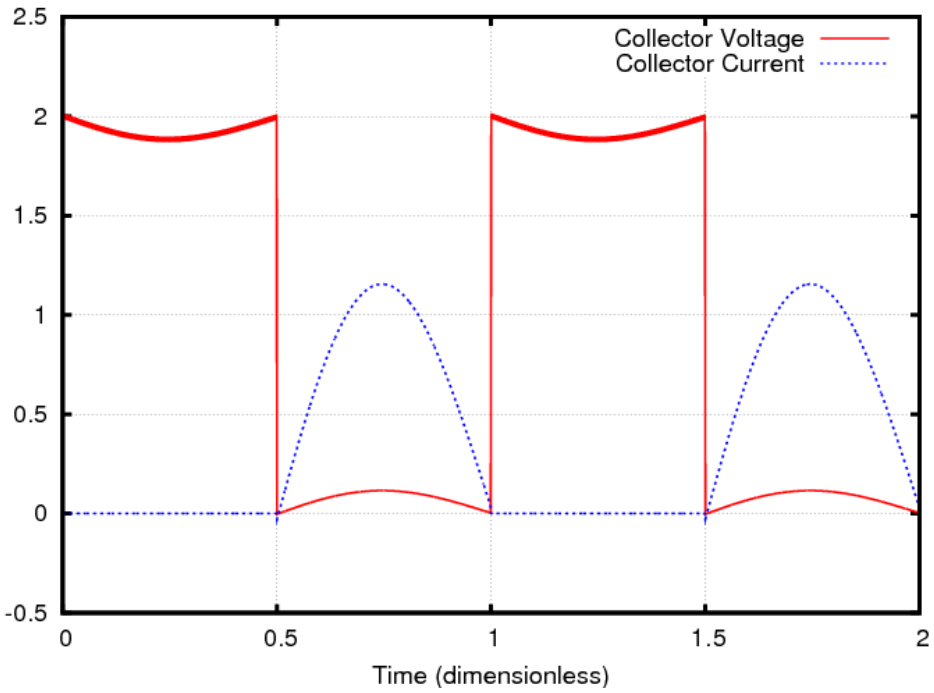

Figure 3: Upper transistor waveforms for amplifier in Figure 1 (voltage mode). Blue is the collector voltage and red is the collector current. V_{CC} = 1. Effects of finite transistor "on" resistance are seen in the blue curve "humps" during the transistor on times (the collector-emitter voltage drop).

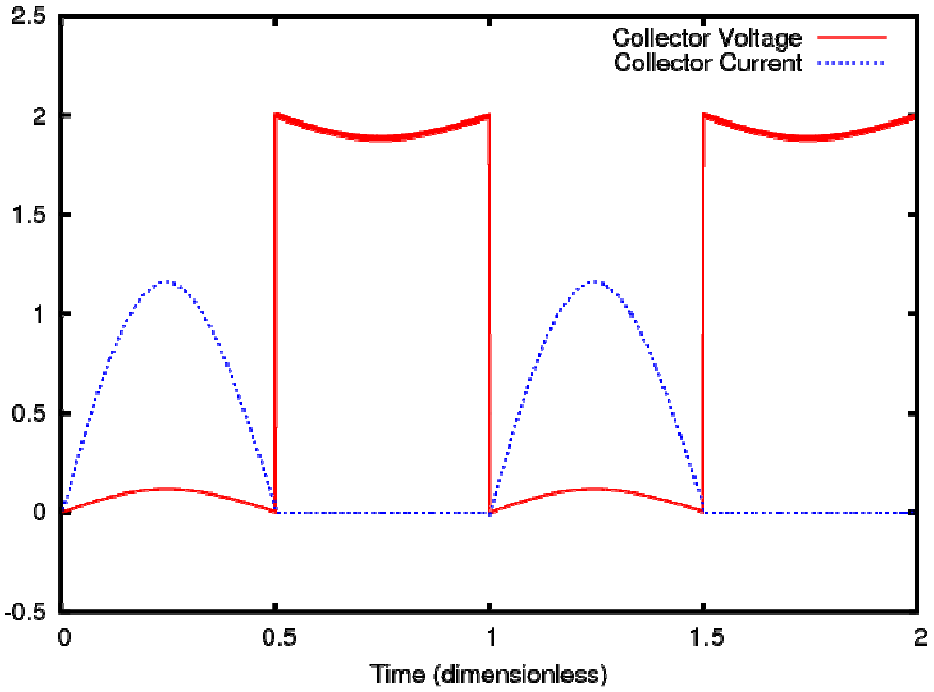

Figure 4: Class-D lower transistor collector voltage (blue) and current (red) waveforms. Note the 180 degree phase shift with respect to Figure 3.

Keeping the "on" resistance low and minimizing the duration of switching transitions are important ways of enhancing efficiency. This mode of operation is very useful in switch-mode power supplies and switching audio amplifiers. Using very fast HEMTS, Class-D can be made to work up to 1-2GHz. However, as frequency rises, problems arise when the transistors behave less like ideal switches as a result of their finite switching times. Namely, as the operating frequency moves up on the transistors gain/frequency curve, losses and other non-idealities become much more significant. For this reason, cleverer methods are needed to reduce switching element losses when the switches are no longer ideal. This is where Class-E and Class-F become helpful.

Pros:

- Conceptually simple
- Simple to implement
- Possible pulse duty-cycle modulation allows "linear" operation
- Push-pull configuration allows even harmonic cancellation

Cons:

- Efficiency degrades as switching times approach significant fraction of on-off period
- Voltage spikes possible from leakage inductance in poorly coupled transformers: generate losses in switch or protective "snubber" networks
- Considerable harmonic power generation

2.2. Class-E

Class-E is an easily implemented topology
Figure 5) that uses "soft switching" where the capability of the output network to "phase" the collector voltage and current in such a way as to minimize overlap between collector current and voltage curves is used (i.e. transistor switching times and output circuit waveform are coordinated to minimize losses). Notable, and necessary for proper basic class-E operation is the shunt collector capacitor C_p and the collector choke RFC.

The shunt capacitor and the load RLC network are chosen such that during the transistor "off" periods, the voltage across the shunt capacitor rises to about 3.5 times the DC supply voltage and is fully discharged at the end of the transistor "off" period. Specifically, when the transistor switches off rapidly, the choke inductor current cannot change over such a short time span. The choke inductor current will remain essentially constant. The inductor current causes the shunt capacitor to be energized with a "hammer-blow" of charge before dumping this stored energy into the load network. The transistor then switches back on when the shunt capacitor voltage vanishes, drawing current through the choke inductor and the process repeats itself in the next cycle.

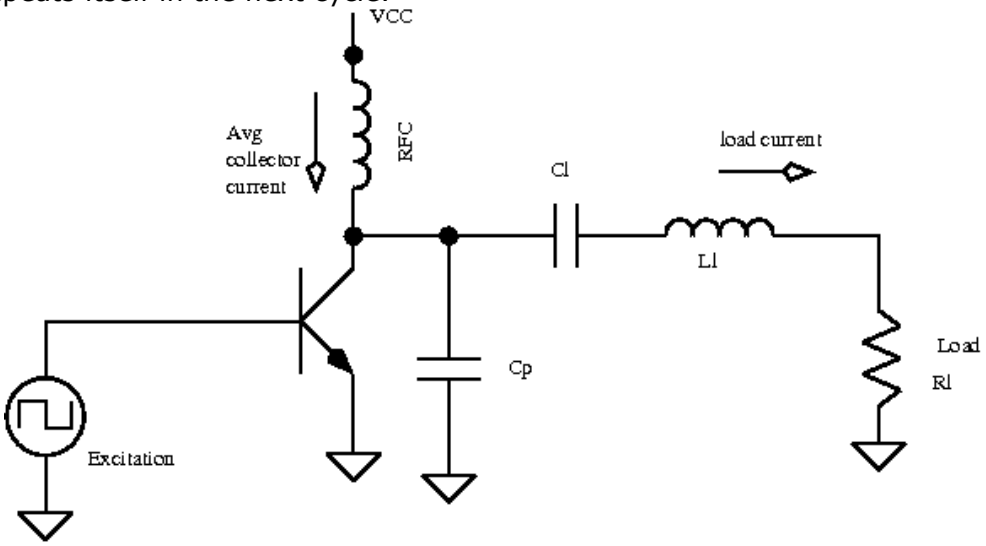

Figure 5: Simplified Class-E amplifier

Mathematically, Class-E operation is defined by the collector voltage and its time derivative vanishing at the transistor turn-on time. This is observed in
Figure 6 as a smooth tailing-off on the right-hand side of the red collector voltage pulses.

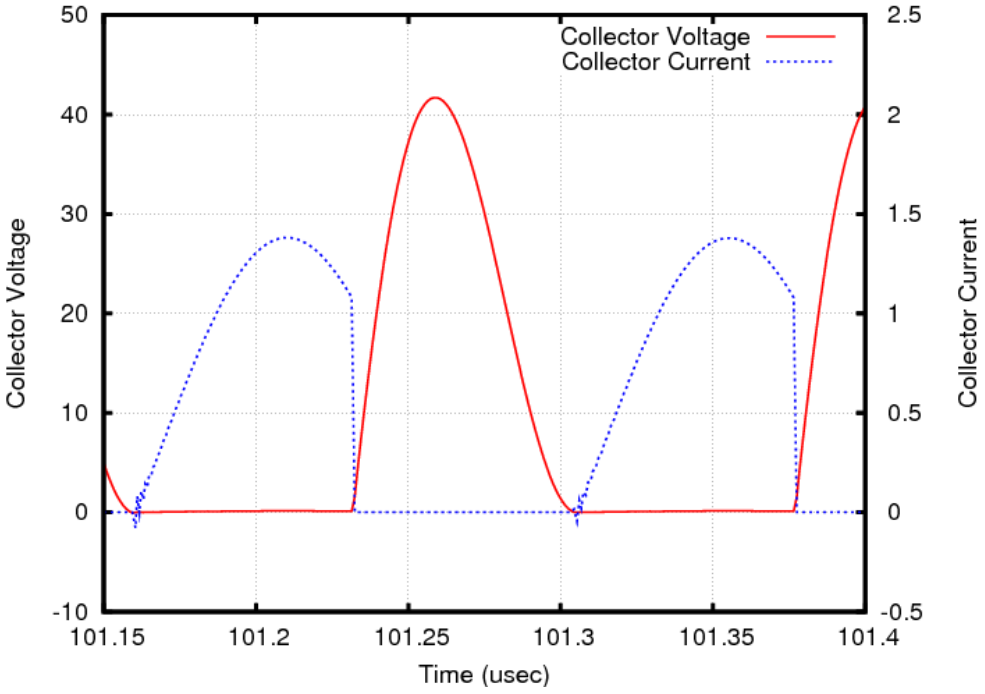

Figure 6: Voltage and current on the drain

Furthermore, the transistor collector-emitter voltage is zero (or at a minimum) when the transistor turns off. This is known as "zero-voltage switching" or ZVS. The current is not necessarily zero, as we see in the ideal Class-E current curve (blue) in Figure 6.

Since we have no overlap of transistor current and voltage curves, the efficiency of this idealized case is 100%. The output RLC network is generally a low to medium-Q (Q≈10) circuit tuned below resonance such that the impedance at the fundamental frequency appears inductive and all harmonics above the fundamental "see" nearly an open circuit on the load network (not including the shunt capacitor).

The choice of switch duty-cycle, DC collector voltage and load circuit are all connected and there is much flexibility in designing matching and filter networks. The shunt collector capacitance (of which the transistor parasitic capacitance is a part) defines the maximum permissible frequency where Class-E operation can be achieved. If C_p is too large, no combination of series load elements will be able to achieve Class-E waveforms on the collector.

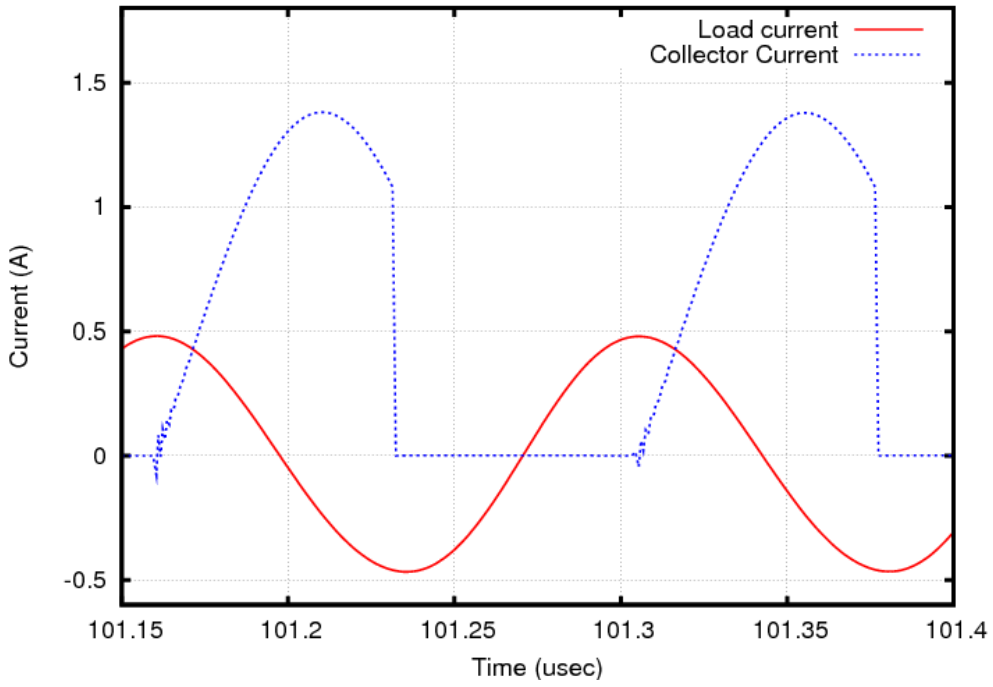

Figure 7: Comparison of the load and drain currents

Practical Class-E amplifiers cannot achieve 100% efficiency because switching delays and parasitic losses in the switching devices and passive components dissipate power. Despite this, efficiencies exceeding 90% are possible if fast switching devices are used (transition times < 10-20% of on-off period) and careful attention is given to external component loss minimization. Keep in mind that class-E operation has a problem common with reduced-conduction angle amplifiers (Class-C), i.e. Class-E stage can exhibit low gain. Use high-gain-bandwidth device so efficiencies are not wiped out by the need for high-level drive signals. Input signal conditioning can help improve Class-E amplifier gain as well (usually by "squaring up" the input base/gate signal and facilitating power transfer to the input with impedance matching, e.g. a transformer).

Pros:

- Simple topology
- High efficiency possible
- Reasonable bandwidth
- Can be collector/drain modulated for envelope restoration linearization
- Output network provides some harmonic filtering

Cons:

- Can suffer low gain, high level input signal often required
- Collector voltage spike can cause switching device breakdown
- Switching device package parasitics complicate design of output network at microwave frequencies.

2.3. Class-F

Another method to achieve a "collector voltage-current non-overlapping" condition is to short-circuit all even harmonics and open-circuit all odd harmonics while allowing power flow to the load only for the fundamental. This "squares-up" the collector voltage waveform making the voltage transitions steep and the current is zero precisely when the switch opens and closes. This "zero-current" or ZCS switching condition and gives rise to Class-F operation.

Figure 8 illustrates a conceptual schematic for the Class-F. The key to its operation is the ¼ wave (at the fundamental) transmission line that connects the collector to an AC short to ground (the bypass capacitor). At the fundamental and all odd harmonics of the fundamental, the collector side of this transmission line looks like an open circuit. For all even harmonics, the collector has a harmonic short circuit to ground.

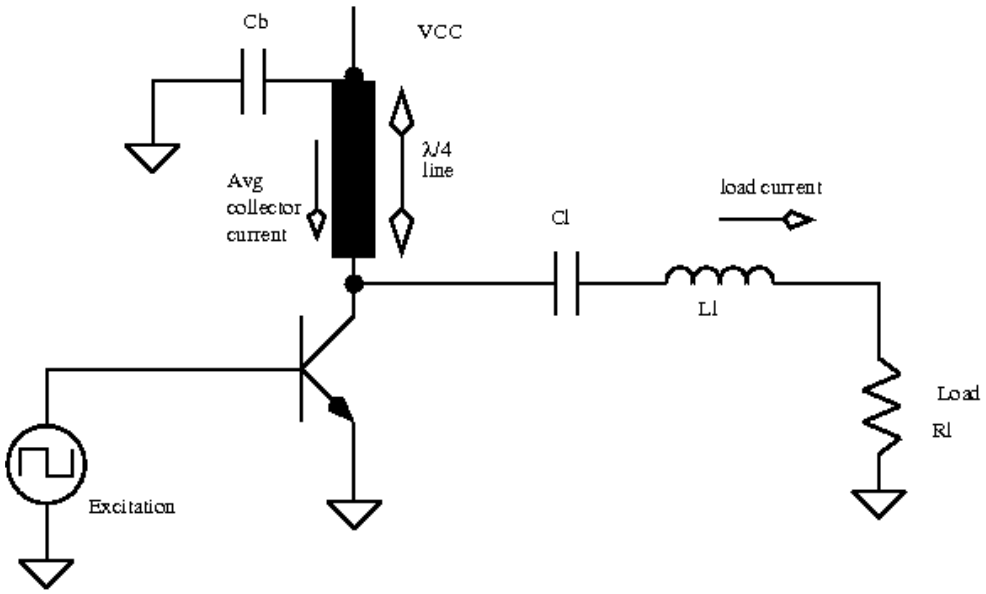

Figure 8: Simplified Class-F topology

The resonant RLC circuit is tuned to the fundamental operating frequency (i.e. at resonance, the impedance at the fundamental takes a purely resistive value R_l.)

Simulations are carried out where we have allowed 10% resistive loss in the transistor during its "on" state.

Figure 9 shows the resulting collector voltage and current waveforms. Note the steep voltage transitions that are the result of the high levels of odd-harmonic signal content in the collector circuit. Current-voltage curve overlap is minimal and represents the small series "on" resistance losses in the transistor that was simulated.

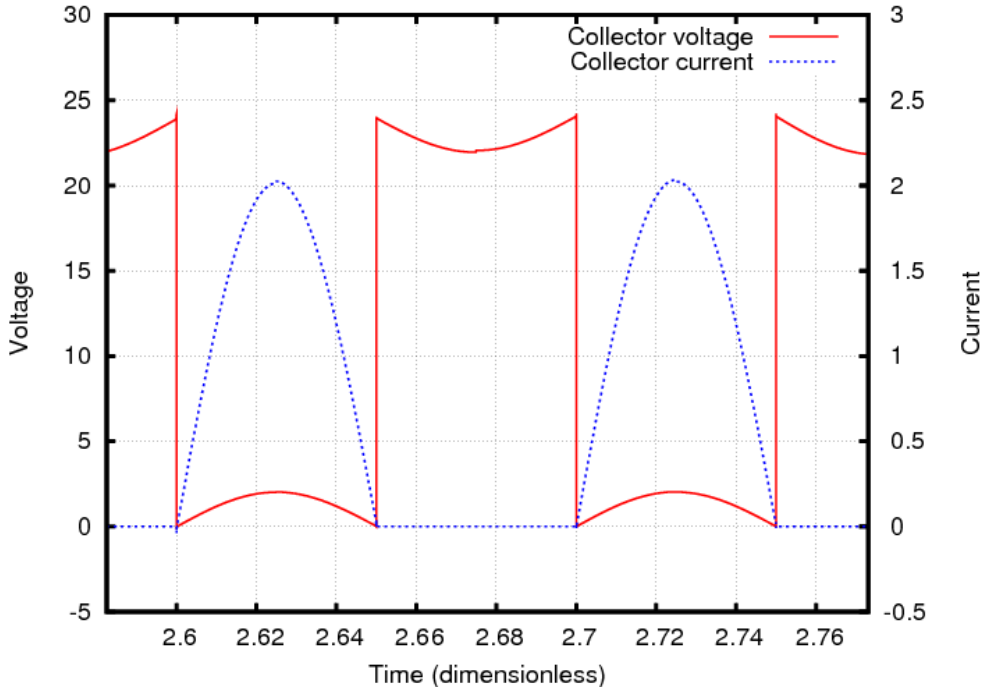

Figure 9: Class F collector waveforms for voltage and current

The simulation results for the current on the DC supply side in
Figure 10 show a combination of even and odd harmonic components (blue curve) along with a DC component. Physically speaking, this DC current component from the supply is the only component that supplies energy to the amplifier. The supply side current harmonics do (almost) no real work in the system and only represent reactive energy "sloshing around" in the ¼ wave transmission line element. The output signal (red curve) is a well-behaved sinusoid as a result of the filtering provided by the output RLC network.

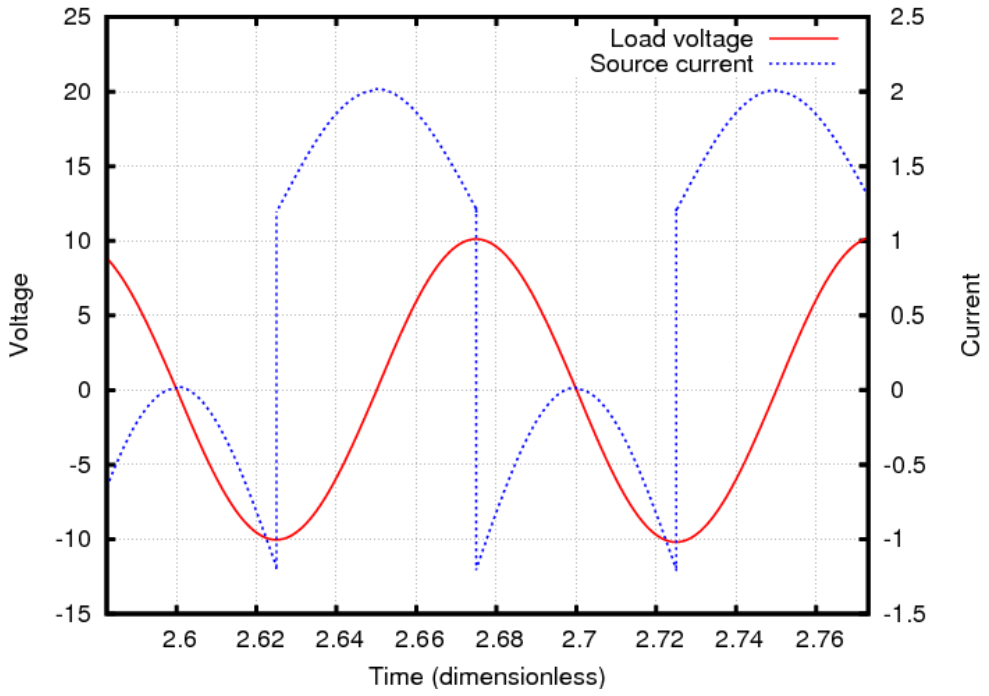

Figure 10: Load voltage and current from power supply

Practical implementations of Class-F amplifiers often rely on the peaking of a few of the odd harmonics to increase the slope of the collector voltage, thereby minimizing switching transition losses. At "low" frequencies, these peaking resonant networks can be constructed using lumped components. At microwave frequencies, distributed transmission-line elements are used. The challenge comes from devising a practical harmonic trap/short that treats as many harmonics as possible while keeping circuit complexity and parasitic losses to a minimum.

Pros:

- Conceptually simple idea
- Voltage "spikes" of Class-E not present. Switch breakdown less likely.

Cons:

- Practical implementations can become complicated as practical harmonic shorts/opens do not behave like the ideal λ/4 transmission line in
- Figure 8 used in the simulation.
- Device parasitics complicate design (especially the collector/drain capacitance that proved so useful in Class-E designs) and reduce efficiency.

2.4. Inverse Class-F

Inverse Class-F amplifiers utilize even harmonic peaking to "square-up" the current waveform in order to achieve high efficiency. Whereas the Class-F uses an odd-harmonic "open"/even-harmonic "short" to generate a squared-up collector voltage waveform, the Inverse Class-F shorts out the odd harmonics while presenting the collector with an even harmonic open circuit.

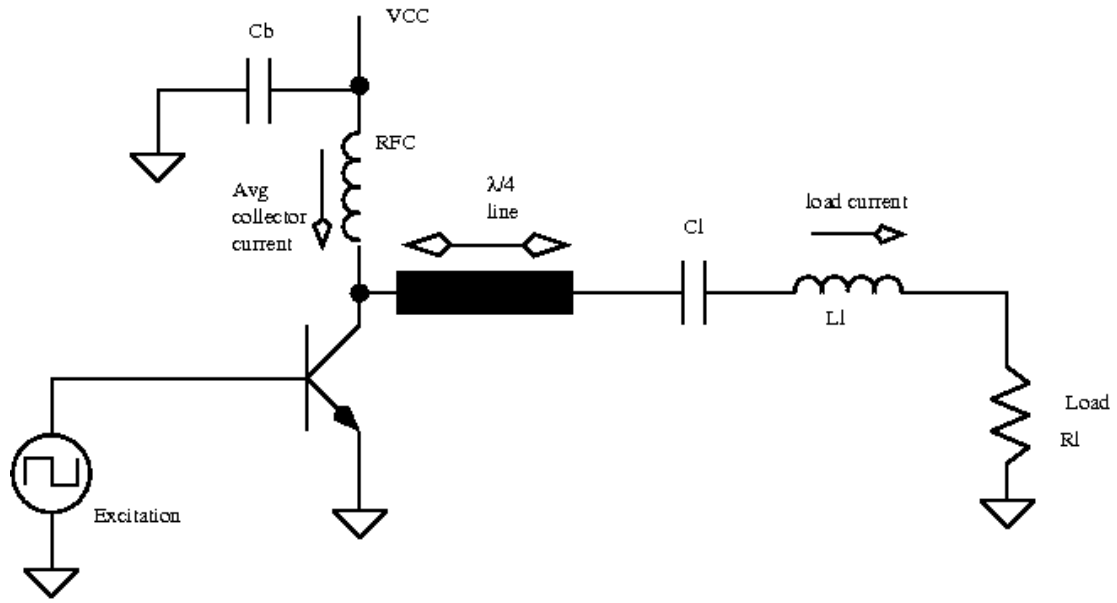

Figure 11: Simplified method for generating Inverse Class-F operation using a 1/4 wave line

In

Figure 11, if we choose the ¼ wave transmission line impedance to be equal to the load resistance at fundamental resonance, the fundamental frequency is passed without any impedance transformation. At the second-harmonic frequency and above, the inductor has a high impedance approaching infinity (in this idealized simulation case). Its impedance transforms to itself on the collector side of the transmission line at even harmonics, where the transmission line is a multiple of ½ a wavelength. At odd harmonics, the inductor's high reactance is transformed to a low impedance (short circuit) at the collector end. Hence, the currents flowing in the transmission line at the collector are rich in odd harmonics, yielding the sharp, square transitions to the collector load current wave.

As a result of this, the waveforms for the collector current and voltage are practically those found in

Figure 9 with the roles of current and voltage interchanged. Instead of the class-F ZCS switching condition, we get the ZVS condition. As in idealized Class-F, the voltage and current waveforms do not overlap (except if the switch exhibits some series “on” resistance, as shown in the Class-F case).

Inverse Class-F finds use in efficient low-voltage monolithic and LDMOS amplifiers where lumped or distributed elements can be used to construct the required harmonic filters. Pros and cons are similar to those of Class-F. Complexity in the output network (particularly if lumped resonators are used) can present practical implementation problems.

3. Summary

Briefly speaking, amplifiers fall into either classes of limited-angle conduction, classical modes (Class A, AB, B and C) or on-off "switchers" where attempts are made to limit losses in the switching device (Class D, E, F, Inverse F). There is a good deal of complicated mathematical analysis that goes into the design and description of these power amplifiers. We have made no attempt at mathematical rigor in this article. Instead, the purpose has been to clarify the definitions as well as to give a qualitative "feel" for how these different amplifiers function.

The present availability of transistors that are capable of extreme switching speeds has made possible high performance, high efficiency and cost effective switching amplifiers that can operate beyond X-band. These high-efficiency switching amplifiers have the potential to push out some vacuum devices from their bastion of high-power transmitters. Of course, to construct amplifiers that operate in the microwave bands requires a far more profound understanding of the effects of parasitics than is presented here, but the basics of operation described in this article are still qualitatively valid.

Building on the presentation from Part I, we add the switching classes to the classical limited conduction angle classes in Table 1.

Class	Type (1)	Linearity	Power Efficiency	Ease for implement.	Power capability	Gain (2)
A	LCA	Excellent	Poor	Very Good	Low	High
B	LCA	Medium	Good	Very Good	High	Medium/ High
AB	LCA	Good	Fair	Good	Medium/ High	High
C	LCA	Poor	Good	Fair	High	Low
D	Switcher	(3)	Very Good	Very Good	High	High
E	Switcher	Poor	Excellent	Good	High	Low/ Medium
F	Switcher	Poor	Excellent	Fair	High	Medium
Inverse F	Switcher	Poor	Excellent	Fair	High	Medium

Table 1: Brief performance comparison between various amplifier classes

Note (1): Active device mode of operation: LCA = Limited conduction angle (non-switching) operation, Switcher = "on-off" operation only.

Note (2): This is strongly dependent on device characteristics and operating frequency. Description is intended to give an idea of drive power needs yielding useful output in typical situations. Actual performance in practical situations will vary.

Note (3): Linear operation can be achieved using pulse-width modulation on the drive signal. However, the class-D amplifier is a non-linear system in the strict sense of the term.

Class	Technology	Frequency	Power	Efficiency
D	LDMOS	1GHz	13W	60.00%
D	RF Si MOSFET	13.56MHz	1.7kW	85.00%
E	LDMOS	1GHz	10W	73.00%
E	RF Si MOSFET	81MHz	300W	82.00%
F	AlGaN/GaN	879MHz	2W	78.00%

Table 2: Some example power and efficiencies

As a final word, the reader may have noticed that Part I and II of our series did not discuss the Doherty amplifier. The reason for this is that the Doherty amplifier does not have a convenient "letter" designation. Furthermore, it is a very special amplifier topology that combines the benefits of the Class AB and Class C amplifiers. Given its relative complexity compared to the letter-classed amplifiers, the Doherty deserves an article devoted to itself.

4. References

4.1. Simulation

All simulations in this article were carried out using Octave 3.0 [1] and/or NGSpice [2] models. The reader is referred to the following websites for more information on these packages.

[1] http://www.gnu.org/software/octave/
[2] http://ngspice.sourceforge.net/

4.2. General Reading

The reader is who wishes a more in-depth treatment of the subject of RF and microwave power amplifiers can consult some of the works used in the preparation of this article.

[3] S. C. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 1999.
[4] A. Grebennikov and N. O. Sokal, Switchmode RF Power Amplifiers, Elsevier/Newnes, 2007.
[5] W. Gerhard and R. Knöchel, "A 2.14 GHz inverse class-F Si-LDMOS power amplifier with voltage second-harmonic peaking," *Proc. German Microwave Conf.,* Mar. 2006.
[6] N. O. Sokal, "Class-E RF power amplifiers," *QEX,* pp. 9-20, Jan.-Feb. 2001. (Online at: http://www.arrl.org/tis/info/pdf/010102qex009.pdf)